REMARKS

New claims 51-54 are added. The new claims are supported by the originally-filed application by exemplary shown embodiments in Figs. 3 and 7. Claims 34-40 and 44-54 remain in the application. Reconsideration of the application in view of the amendments and the remarks to follow is requested.

Figure 3 is amended to correct a typographical error. Support for the correction is disclosed at page 6 of the originally-filed application and Figure 2.

Claims 34-37 and 44-46 stand rejected under 35 U.S.C. §102(e) as being anticipated by Liaw et al. (5,960,276). Claims 37, 39-40 and 47-50 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Liaw et al. and further in view of Sunouchi et al. (6,294,422). Claims 38 and 39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Liaw et al. and Sunouchi et al. and Lu et al. (6,107,134).

Regarding the anticipation rejection against claim 34 based on Liaw, such claim recites a plurality of active areas having widths defined by shallow trench isolation regions of no greater than about one micron, at least some of the widths being different; and gate lines disposed over the plurality of active areas to provide individual transistors, those transistors whose widths are different having different threshold voltages from one another. Liaw teaches narrow active area 12N with a "width between 0.4 and 1.0μm" and a wide active area 12W with a "width greater than 1.0μm" (col. 2, lines 1-8; Figs. 1-2), that is, the combination of Liaw active areas include one width that is greater than 1.0μm. Therefore, it is inconceivable that Liaw teaches or suggests a plurality of active

areas having widths of **no greater** than about one micron as positively recited in claim 34. Claim 34 is allowable.

Moreover, the claim 34 recitation to those transistors whose widths (defined by shallow trench isolation regions) are different having different threshold voltages from one another is not taught nor suggested by Liaw. The Examiner refers to Liaw, Fig. 4 and a Table located at col. 4, lines 9-25, to allege teaching of this limitation, and then the Examiner correctly states Liaw teaches a correlation between **channel widths** and threshold voltages. Channel widths of Liaw are not transistor widths (defined by shallow trench isolation regions) as recited in claim 34. The channel width of Liaw is defined as, "conductive gates 40 have a channel width 42" (col. 4, lines 1-2) and is clearly shown at Fig. 3B (referenced as 42) as a dimension perpendicular to dimensions "defined by shallow trench isolation regions" (see active areas 12N and 12W, Figs. 1-2 of Liaw). In no fair or reasonable interpretation does the channel width of Liaw teach or suggest **transistors** whose widths are different having different threshold voltages as positively recited in claim 34. Liaw fails to teach or suggest a positively recited limitation of claim 34, and therefore, claim 34 is allowable.

Claims 35-40 and 51 depend from independent claim 34, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not shown or taught by the art of record.

Regarding the rejection against claim 37, it is unclear if the claim is rejected as being anticipated by Liaw or as being obvious over Liaw and Sunouchi. However, the claim recites one of the individual transistors comprises a portion of precharge circuitry, and neither reference teaches precharge circuitry. An electronic search of the references verifies this, and notably, the Examiner does not provide any teachings from either reference to precharge circuitry (pgs. 3-5 of paper no. 14). Therefore, the combination of Liaw and Sunouchi, singularly or in any combination, fails to teach or suggest one of the individual transistors comprises a portion of precharge circuitry as positively recited in claim 37. Claim 37 is allowable.

Regarding the rejection against claim 38, such claim recites one of the individual transistors comprises a pass transistor. The Examiner correctly states that Liaw and Sunouchi do not teach such limitation and relies on Lu (pg. 6 of paper no. 14). The motivational rationale for the combination is stated as, it would be obvious to include the pass circuitry of Lu within the Sunouchi DRAM circuitry since Lu teaches pass circuitry is peripheral circuitry which is typically found within DRAM devices (pg. 6 of paper no. 14). Respectfully, the Examiner is effectively stating that since you can modify the Sunouchi invention by the teachings of Lu, it is obvious to do so. The Examiner is respectfully reminded that the mere fact that references <u>can</u> be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. MPEP §2143.01 (8th edition) *citing In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Although a prior art device

"may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so". 916 F.2d at 682, 16 USPQ2d at 1432; MPEP §2143.01; See also *In re Finch,* 972 F.2d, 1260, 23 USPQ2d, 1780 (Fed. Cir. 1992). The Examiner has failed to provide any desirability for modifying the Sunouchi invention to include pass circuitry, and has merely stated you can because pass circuitry is periphery circuitry and periphery circuitry "is typically found within DRAM devices". Pursuant to the above authority, this is inappropriate, and therefore, the obviousness rejection against claim 39 fails. Claim 39 is allowable.

Regarding the anticipation rejection against claim 44 based on Liaw, such claim recites individual active sub-areas having respective widths and defining, in part, separate transistors, wherein each of the separate transistors has a different threshold voltage. Liaw teaches a correlation between **channel widths** and threshold voltages (Figs. 3B and 4; Table located at col. 4, lines 9-25) and fails to teach ir suggest any correlation between active sub-areas widths **and** threshold voltages. Accordingly, it is inconceivable that Liaw teaches or suggests individual active sub-areas having respective widths and defining, in part, separate transistors, wherein each of the separate transistors has a different threshold voltage as positively recited in claim 44. Claim 44 is allowable.

Claims 45-48 and 52 depend from independent claim 44, and therefore, are allowable for the reasons discussed above with respect to the independent

claim, as well as for their own recited features which are not shown or taught by the art of record.

Regarding the obviousness rejection against claim 49 based on Liaw and Sunouchi, such claim recites a plurality of transistors being joined in a parallel configuration to provide a pull down circuit coupled to a common node. The references fail to teach or suggest a pull down circuit. Electronic searches verify such limitation is not recited in the references. Notably, the Examiner fails to point to any teachings of the references to such positively recited limitation of claim 49. Accordingly, Liaw and Sunouchi, singularly or in any combination, fails to teach or suggest a positively recited limitation of claim 49. Claim 49 is allowable.

Moreover, claim 49 recites a plurality of transistors being joined in a parallel configuration to provide a pull down circuit coupled to a common node. One skilled in the art understands this recitation is referring to a parallel **circuit**, not parallel oriented **structure** such as word lines formed in parallel rows. The Examiner correctly states that Liaw fails to teach such limitation and relies on Sunouchi (pg. 5 of paper no. 14). However, Sunouchi teaches transistors formed structurally parallel to one another (abstract; Figs. 34 and 37), but fails to teach or suggest a parallel circuit. Accordingly, the combination of Liaw and Sunouchi fails to teach or suggest, singularly or in any combination, a plurality of transistors being joined in a parallel configuration to provide a pull down circuit

coupled to a common node. Since a positively recited limitation of claim 49 is not taught or suggested, claim 49 is allowable.

Additionally, claim 49 recites individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is less than the one width. Liaw teaches at least one active area having a width greater than one micron (col. 2, lines 1-8; Figs. 1-2) and Sunouchi does not teaches dimensions of active areas. Accordingly, it is inconceivable that the combination or art teaches or suggests individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is less than the one width as positively recited by claim 49. Claim 49 is allowable.

Claims 50 and 53-54 depend from independent claim 49, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not shown or taught by the art of record.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 9-8-03

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